

Description

The 74LVC1G08 is a single 2-input positive AND gate with a standard totem pole output. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

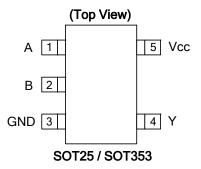
The gate performs the positive Boolean function:

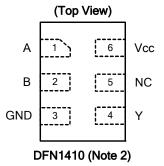
$$Y = A \bullet B \text{ or } Y = \overline{A + B}$$

Features

- Wide Supply Voltage Range from 1.65 to 5.5V
- ± 24mA Output Drive at 3.3V
- CMOS low power consumption
- I_{OFF} Supports Partial-Power-Down Mode Operation
- Inputs accept up to 5.5V
- ESD Protection Tested per JESD 22
 Exceeds 200-V Machine Model (A115-A)
 Exceeds 2000-V Human Body Model (A114-A)
- · Latch-Up Exceeds 100mA per JESD 78, Class II
- · Range of Package Options
- · Direct Interface with TTL Levels
- SOT25, SOT353, and DFN1410: Assembled with "Green" Molding Compound (no Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

Pin Assignments





Applications

- Voltage Level Shifting
- · General Purpose Logic
- Wide array of products such as.
 - PCs, networking, notebooks, netbooks, PDAs
 - o Computer peripherals, hard drives, CD/DVD ROM
 - o TV, DVD, DVR, set top box
 - Cell Phones, Personal Navigation / GPS
 - o MP3 players ,Cameras, Video Recorders

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

2. Pin 2 and pin 5 of the DFN1410 package are internally connected.



Pin Descriptions

Pin Name	Description			
Α	Data Input			
В	Data Input			
GND	Ground			
Y	Data Output			
Vcc	Supply Voltage			
NC	No Connection			

Logic Diagram



Function Table

Inp	Output	
Α	В	Y
Н	Н	Н
L	Х	L
X	L	L



Absolute Maximum Ratings (Note 3)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	200	V
V _{CC}	Supply Voltage Range	-0.5 to 6.5	V
VI	Input Voltage Range	-0.5 to 6.5	V
Vo	Voltage applied to output in high impedance or I _{OFF} state	-0.5 to 6.5	V
Vo	Voltage applied to output in high or low state.	-0.3 to V _{CC} +0.5	V
l _{IK}	Input Clamp Current V _I <0	-50	mA
I _{OK}	Output Clamp Current	-50	mA
Io	Continuous output current	±50	mA
	Continuous current through Vdd or GND	±100	mA
TJ	Operating Junction Temperature	-40 to 150	°C
T _{STG}	Storage Temperature	-65 to 150	°C

Notes: 3. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.



Recommended Operating Conditions (Note 4)

Symbol		Parameter	Min	Max	Unit
\/	Operating Voltage	Operating	1.65	5.5	V
V _{CC}	Operating voltage	Data retention only	1.5		V
		V _{CC} = 1.65V to 1.95V	0.65 X V _{CC}		
	High-level Input Voltage	V _{CC} = 2.3V to 2.7	1.7		V
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6V	2		V
		V _{CC} = 4.5V to 5.5V	0.7 X V _{CC}		
		V _{CC} = 1.65V to 1.95V		0.35 X V _{CC}	
	l avy laval innyt valtage	V _{CC} = 2.3V to 2.7V		0.7	V
V_{IL}	Low-level input voltage	V _{CC} = 3V to 3.6V		0.8	V
		V _{CC} = 4.5V to 5.5V		0.3 X V _{CC}	
VI	Input Voltage		0	5.5	V
Vo	Output Voltage		0	V _{CC}	V
		V _{CC} = 1.65V		-4	
		V _{CC} = 2.3V		-8	
I _{OH}	High-level output current	V/ 2V/		-16	mA
		$V_{CC} = 3V$		-24	
		V _{CC} = 4.5V		-32	
		V _{CC} = 1.65V		4	
		V _{CC} = 2.3V		8	
I_{OL}	Low-level output current	V2V		16	mA
		$V_{CC} = 3V$		24	
		$V_{CC} = 4.5V$		32	
		$V_{CC} = 1.8V \pm 0.15V, 2.5V \pm 0.2V$		20	
Δt/ΔV	Input transition rise or fall rate	$V_{CC} = 3.3V \pm 0.3V$		10	ns/V
		$V_{CC} = 5V \pm 0.5V$		5	
T _A	Operating free-air temperature		-40	85	°C

Notes: 4. Unused inputs should be held at Vcc or Ground.



Electrical Characteristics (All typical values are at Vcc = 3.3V, T_A = 25°C)

Over recommended free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Vcc	Min	Тур.	Max	Unit
		I _{OH} = -100 μA	1.65V to 5.5V	V _{CC} – 0.1			
		I _{OH} = -4 mA	1.65V	1.2			
	High Level Output	I _{OH} = -8 mA	2.3V	1.9			.,
V_{OH}	Voltage	I _{OH} = -16 mA	21/	2.4			V
		I _{OH} = -24 mA	3V	2.3			
		I _{OH} = -32 mA	4.5V	3.8			
		I _{OL} = 100 μA	1.65V to 5.5V			0.1	
		I _{OL} = 4 mA	1.65V			0.45	
	High lovel lange Valtage	I _{OL} = 8 mA	2.3V			0.3	.,
V_{OL}	High-level Input Voltage	I _{OL} = 16 mA	01/			0.4	V
		I _{OL} = 24 mA	3V			0.55	
		I _{OL} = 32 mA	4.5V			0.55	
II	Input Current	V _I = 5.5V or GND	0 to 5.5V			± 5	μA
I _{OFF}	Power Down Leakage Current	V_I or $V_O = 5.5V$	0			± 10	μΑ
Icc	Supply Current	$V_I = 5.5V$ of GND $I_O=0$	1.65V to 5.5V			10	μΑ
ΔI _{CC}	Additional Supply Current	One input at V _{CC} – 0.6 V Other inputs at V _{CC} or GND	3V to 5.5V			500	μA
Ci	Input Capacitance	$V_i = V_{CC} - \text{or GND}$	3.3		4		pF
	The word Decistors	SOT25	(Note 5)		204		°C/W
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT353	(Note 5)		371		°C/W
		DFN1410	(Note 5)		430		°C/W
	Thermal Resistance	SOT25	(Note 5)		52		°C/W
θ_{JC}	Junction-to-Case	SOT353	(Note 5)		143		°C/W
		DFN1410	(Note 5)		190		°C/W

Notes: 5. Test condition for SOT25, SOT353, and DFN1410: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.



Switching Characteristics

Over recommended free-air temperature range, CL = 15pF (see Figure 1)

Parameter	From	TO		Vcc = 1.8 V ± 0.15V		2.5 V .2V	Vcc = ± 0	3.3 V .3V		= 5 V 0.5V	Unit
	(Input)	(OUTPUT)	Min	Max	Min	Max	Min	Max	Min	Max	
t _{pd}	A or B	Y	1.5	7.2	0.7	4.4	0.8	3.6	0.8	3.4	ns

Over recommended free-air temperature range, CL = 30 or 50pF as noted (see Figure 2)

Parameter	From	TO	Vcc = ± 0.	1.8 V 15V	Vcc = ± 0	2.5 V 2.2V	Vcc = ± 0	3.3 V .3V		= 5 V 0.5V	Unit
	(Input)	(OUTPUT)	Min	Max	Min	Max	Min	Max	Min	Max	
t _{pd}	A or B	Y	2.4	8.0	1.1	5.5	1.0	4.5	1.0	4.0	ns

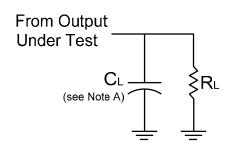
Operating Characteristics

 $T_A = 25 \, {}^{\circ}C$

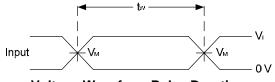
	Parameter	Test Conditions	Vcc = 1.8 V	Vcc = 2.5 V	Vcc = 3.3 V	Vcc = 5 V	Unit
C _{pd}	Power dissipation capacitance	f = 10 MHz	21	24	26	31	pF



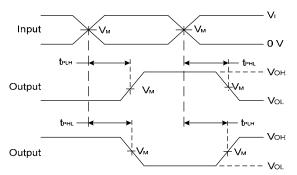
Parameter Measurement Information



Vcc	In	puts	V _M	CL	R_L
700	VI	t _r /t _f	▼ IVI	OL	IXL
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	15pF	1ΜΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	15pF	1ΜΩ
3.3V±0.3V	3V	≤2.5ns	1.5V	15pF	1ΜΩ
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	15pF	1ΜΩ



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

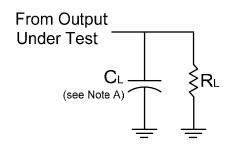
Figure 1. Load Circuit and Voltage Waveforms

Notes: A. Includes test lead and test apparatus capacitance.

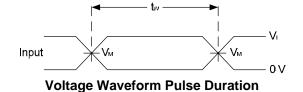
- B. All pulses are supplied at pulse repetition rate \leq 10 MHz.
- C. Inputs are measured separately one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{PD}.

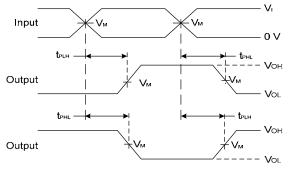


Parameter Measurement Information (Continued)



Vcc	Inj	outs	V _M	CL	R_L
700	VI	t _r /t _f	▼ IVI	O _L	IXL
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	30pF	1ΚΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	30pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	50pF	500Ω





Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

Figure 2. Load Circuit and Voltage Waveforms

Notes: A. Includes test lead and test apparatus capacitance.

- B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
- C. Inputs are measured separately one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as $t_{\text{PD.}}$



Ordering Information

 74LVC1G 08 XXX - 7

 Logic Device
 Function
 Package
 Packing

 74 : Logic Prefix
 08 : 2-Input
 W5 : SOT25
 7 : Tape & Reel

 LVC : 1.65 to 5.5V
 AND-Gate
 SE : SOT353

 Family
 FZ4 : DFN1410

1G: One gate

Device	Package Packaging		7" Tape and Reel		
Device	Code	(Note 6)	Quantity	Part Number Suffix	
74LVC1G08W5-7	W5	SOT25	3000/Tape & Reel	-7	
74LVC1G08SE-7	SE	SOT353	3000/Tape & Reel	-7	
74LVC1G08FZ4-7	FZ4	DFN1410	5000/Tape & Reel	-7	

Notes: 6. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.



Marking Information

(1) SOT25 and SOT353

(Top View)

5 4 xx y w x

2

1

XX: Identification code

Y: Year 0~9

<u>W</u>: Week: A~Z: 1~26 week;

a~z: 27~52 week; z represents

52 and 53 week

 \underline{X} : A $^{\sim}$ Z: Internal code

Part Number	Package	Identification Code
74LVC1G08W5	SOT25	UV
74LVC1G08SE	SOT353	UV

(2) DFN1410

(Top View)

 XX: Identification Code

Y: Year: 0~9

 \overline{W} : Week : A~Z : 1~26 week;

a~z: 27~52 week; z represents

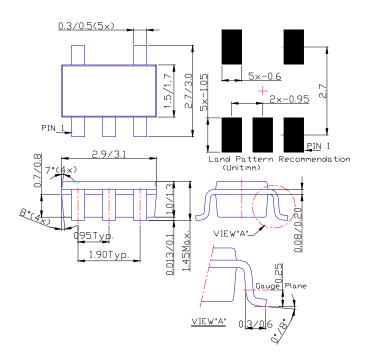
52 and 53 week X: A~Z: Internal code

Part Number	Package	Identification Code
74LVC1G08FZ4	DFN1410	UV

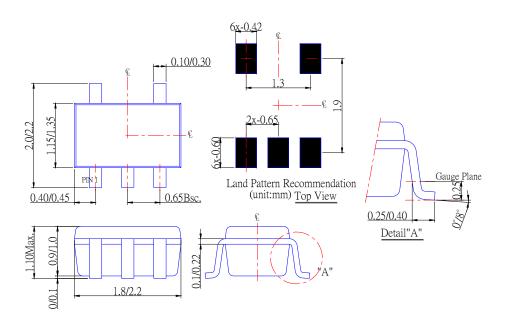


Package Outline Dimensions (All Dimensions in mm)

(1) Package Type: SOT25



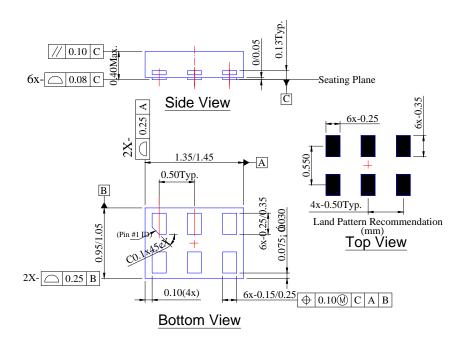
(2) Package Type: SOT353





Package Outline Dimensions (Continued)

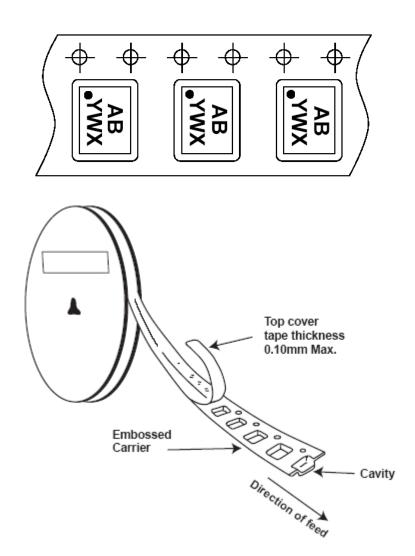
(3) Package Type: DFN1410





Taping Orientation (Note 7)

For DFN1410



Notes: 7. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf



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